Amendments to the Claims

Listing of Claims:

Original Claims 1-12 (canceled).

Claim 13 (new). A control unit for activating an occupant protection device in a motor vehicle, the control unit comprising:

a first arithmetic unit supplying a clock signal and having a first pulse count comparator unit with an input and an output, a first resetter with an input and an output, and a reset input, said output of said first pulse count comparator unit being connected to said input of said first resetter;

a second arithmetic unit supplying a clock signal and having a second pulse count comparator unit, a second resetter, and a reset input connected directly or indirectly to said output of said first resetter, said second pulse count comparator unit having an input and an output, said second resetter having an input connected to said output of said second pulse count comparator unit and said second resetter having an output connected directly or indirectly to said reset input of said first arithmetic unit;

an activating unit supplying a clock signal;

said first arithmetic unit, said second arithmetic unit and said activating unit being

respectively clocked asynchronously relative to one another;

a first logical AND gate having an input side receiving both the clock signal of said first arithmetic unit and the clock signal of said activating unit and having an output feeding an output signal to said input of said second pulse count comparator unit;

a second logical AND gate having an input side receiving both the clock signal of said second arithmetic unit and the clock signal of said activating unit, said second logical AND gate having an output feeding an output signal to said input of said first pulse count comparator unit;

said first resetter resetting said second arithmetic unit by outputting a first reset signal if said first pulse count comparator unit detects an inadmissible number of pulses per unit of time in the output signal of said second AND gate; and

said second resetter resetting said first arithmetic unit by outputting a second reset signal if said second pulse count comparator unit detects an inadmissible number of pulses per unit of time in the output signal of said first AND gate.

Claim 14 (new). The control unit according to claim 13, which further comprises:

first and second logical OR gates;

said output of said second resetter being connected indirectly through said second OR gate to said reset input of said first arithmetic unit;

said output of said first resetter being connected indirectly through said first OR gate to said reset input of said second arithmetic unit;

said first resetter resetting said second arithmetic unit by outputting a first reset signal indirectly through said first OR gate if said first pulse count comparator unit detects an inadmissible number of pulses per unit of time in the output signal of said second AND gate; and

said second resetter resetting said first arithmetic unit by outputting a second reset signal indirectly through said second OR gate if said second pulse count comparator unit detects an inadmissible number of pulses per unit of time in the output signal of said first AND gate.

Claim 15 (new). The control unit according to claim 13, wherein:

said activating unit has a reset input;

at least one of said first and second resetters is connected directly or indirectly to said reset input of said activating unit;

said first resetter resets said activating unit by outputting a first activator reset signal if said first pulse count comparator unit detects an inadmissible number of pulses per unit of time in the output signal of said second AND gate,

and/or

said second resetter resets said activating unit by outputting a second activator reset signal if said second pulse count comparator unit detects an inadmissible number of pulses per unit of time in the output signal of said first AND gate.

Claim 16 (new). The control unit according to claim 13, which further comprises:

a third logical AND gate having an input side receiving the clock signal of said first arithmetic unit and the clock signal of said second arithmetic unit, said third logical AND gate supplying an output signal to both said input of said first pulse count comparator unit and said input of said second pulse count comparator unit;

said first resetter resetting said second arithmetic unit by outputting a first reset signal if said first pulse count comparator unit detects an inadmissible number of pulses per unit of time in the output signal of said third AND gate; and

said second resetter resetting said first arithmetic unit by outputting a second

reset signalif said second pulse count comparator unit detects an inadmissible number of pulses per unit of time in the output signal of said third AND gate.

Claim 17 (new). The control unit according to claim 14, wherein:

said first arithmetic unit has a first watchdog output;

said activating unit has a watchdog input connected to said first watchdog output, and said activating unit has an arithmetic unit resetting output connected directly or indirectly through said second OR gate to said reset input of said first arithmetic unit; and

said activating unit outputs an arithmetic unit resetting signal directly or indirectly through said second OR gate to said reset input of said first arithmetic unit if said activating unit receives an inadmissible watchdog signal from said first watchdog output.

Claim 18 (new). The control unit according to claim 14, wherein:

said second arithmetic unit has a second watchdog output;

said activating unit has a signal input connected to said second watchdog output, and said activating unit has an arithmetic unit resetting output connected directly or indirectly through said first OR gate to said reset input of said second

arithmetic unit; and

said activating unit outputs an arithmetic unit resetting signal directly or indirectly through said first OR gate to said reset input of said second arithmetic unit if said activating unit receives an inadmissible second watchdog signal from said second watchdog output.

Claim 19 (new). A method for monitoring the proper functioning of a control unit, which comprises the following steps:

generating, with a first logical operation, a first combined signal from two respective clock signals of a first arithmetic unit and of an activating unit;

counting, with a second arithmetic unit, a number of pulses of the first combined signal during a time window;

comparing, with the second arithmetic unit, the number of pulses counted with a second reference value stored in a memory of the second arithmetic unit; and

outputting a resetting signal, with the second arithmetic unit, to a first reset input of the first arithmetic unit if the number of pulses counted deviates by more than an admissible extent from the second reference value of the memory of the second arithmetic unit.

Claim 20 (new). The method according to claim 19, which further comprises:

generating, with a second logical operation, a second combined signal from two respective clock signals of the second arithmetic unit and of the activating unit;

counting, with the first arithmetic unit, a number of pulses of the second combined signal during a time window;

comparing, with the first arithmetic unit, the number of pulses counted with a first reference value stored in a memory of the first arithmetic unit; and

outputting a resetting signal, with the first arithmetic unit, to a second reset input of the second arithmetic unit if the number of pulses counted deviates by more than an admissible extent from the first reference value.

Claim 21 (new). The method according to claim 20, which further comprises:

resetting the activating unit with the first arithmetic unit by outputting a first activator reset signal if the first arithmetic unit detects an inadmissible number of pulses per unit of time in the second combined signal;

and/or

resetting the activating unit with the second arithmetic unit by outputting a second

activator reset signal if the second arithmetic unit detects an inadmissible number of pulses per unit of time in the first combined signal.

Claim 22 (new). The method according to claim 20, which further comprises:

generating, with a third logical operation, a third combined signal from the two respective clock signals of the first arithmetic unit and of the second arithmetic unit;

counting a number of pulses of the third combined signal, during a time window, with both the first arithmetic unit and the second arithmetic unit;

comparing, with each of the first arithmetic unit and the second arithmetic unit, the number of pulses counted with a reference value stored in the memory of the first arithmetic unit or in the memory of the second arithmetic unit;

resetting the second arithmetic unit with the first arithmetic unit by outputting a first reset signal if the first arithmetic unit detects, by the comparison with the respective reference value, an inadmissible number of pulses per unit of time in the third combined signal; and

resetting the first arithmetic unit with the second arithmetic unit by outputting a second reset signal if the second arithmetic unit detects, by the comparison with the respective reference value, an inadmissible number of pulses per unit of time

in the third combined signal.

Claim 23 (new). The method according to claim 20, which further comprises:

feeding a first watchdog signal from a first watchdog output of the first arithmetic unit to a first watchdog input of the activating unit and thereupon outputting, from an arithmetic unit resetting output of the activating unit, an arithmetic unit resetting signal to the first reset input of the first arithmetic unit if the first watchdog signal is inadmissible;

and/or

feeding a second watchdog signal from a second watchdog output of the second arithmetic unit to a second watchdog input of the activating unit and thereupon outputting, from the arithmetic unit resetting output of the activating unit, the arithmetic unit resetting signal to the second reset input of the second arithmetic unit if the second watchdog signal is inadmissible.

Claim 24 (new). The method according to claim 21, which further comprises:

providing the control unit as part of an occupant protection system of a motor vehicle;

at least partially deactivating the occupant protection system with one of the two

arithmetic units, after single or multiple resetting of the other of the two arithmetic units or of the activating unit;

and/or

displaying malfunctions of the control unit and the at least partial deactivation of the occupant protection system to a vehicle occupant.

Claim 25 (new). A method for monitoring the proper functioning of a control unit, which comprises the following steps:

providing the control unit according to claim 1;

generating, with a first logical operation, a first combined signal from two respective clock signals of a first arithmetic unit and of an activating unit;

counting, with a second arithmetic unit, a number of pulses of the first combined signal during a time window;

comparing, with the second arithmetic unit, the number of pulses counted with a second reference value stored in a memory of the second arithmetic unit; and

outputting a resetting signal, with the second arithmetic unit, to a first reset input of the first arithmetic unit if the number of pulses counted deviates by more than

an admissible extent from the second reference value of the memory of the second arithmetic unit.